ANIL SHARMA

PROFESSIONAL SUMMARY

- **1+ years** of working experience as an "**ASIC Verification Engineer"** at **PerfectVIPs**.
- Good grip in **OOPs, Randomization** and **Functional Coverage** of **System Verilog.**
- Worked on **AHB back to back multi master multi slave VIP** verification.
- Good knowledge in **Verilog, System Verilog, UVM and Python.**
- Currently Working on Python based **Google Random Instruction Generator RISC-V** and **UFS 2.0 VIP** Development.

PROFESSIONAL EXPERIENCE

- **ASIC Verification Engineer** at **PerfectVIPs Techno Solutions Pvt. Ltd** **July 2019 - Till Date**

PROJECT DETAILS

Project: Google RISC-V RIG (Python Based) **May 2020 – Till Date**

Description: This project involves the conversion of SV/UVM based Random Instruction Generator to a scalable python based RIG.

Roles & Responsibilities:

- Understanding RISC-V core and ISA.
- Developed **basic building block of python RIG source files.**
- Generate the assembly file for RV32I and RV32IMC extensions instruction.
- Compile and Simulate the assembly file in the SPIKE and OVPSim Simulator.
- Integrate the different extensions such as RV32I and RV32IMC
- Working on the implementation of different Interrupt handlers

Languages: Python, git and System Verilog Tools SPIKE, OVPSim

Project: UFS VIP Development (UVM) **May 2020 – Till Date**

Description: This project involves studying of **UFS 2.0 protocol specification**, understanding the **UFS architecture** and **Development of UFS VIP** from Scratch.

Roles & Responsibilities:

- Developed **Test Bench Architecture.**
- Written the Skeleton code for Test Bench Architecture.
- Developed the Host Controller Interface (HCI) of UFS HOST
- Validate the basic read and write operation of NOP UPIU.
- Working on the implementation and validation of rest of the UPIU's.

Languages: System Verilog Methodology: UVM Tools: VCS

Project: AHB back to back VIP verification (UVM) **January 2020 - March 2020**

Description: This project involves studying of **AHB protocol specification**, understanding the **AHB VIP** and **Verification of AHB back to back Multi Master Multi Slave VIP** from Scratch.

Roles & Responsibilities:

- Developed **Test Bench architecture.**
- Written **SLAVE Driver logic** which involves **writing and reading** of **HDATA** and giving response (**HRESP**) back to respective **bus MASTER**.
- Written the arbitration logic for the interconnect to select the particular master agent through **HBUSREQ** and **HGRANTx** signals of AHB.
- Achieved 80% Functional coverage

Languages: System Verilog Methodology: UVM Tools: VCS

Project: Single Clock Synchronous RAM verification (UVM) **November 2019**

Description: This project involves **design & verification** of **single clock synchronous RAM**.

Roles & Responsibilities:

- Developed the **Test Plan**.
- Developed **Test Bench architecture.**
- Developed **UVM environment** for the same and **run different test cases**.
- Achieved 90% Functional Coverage

Languages: Verilog, System Verilog Methodology: UVM Tools: VCS

Project: Full Adder Design and Verification (System Verilog) **October 2019**

Description: This project involves **design & verification** of 4-bit **Full Adder using System Verilog**.

Roles & Responsibilities:

- Design the **DUT** of **4-bit Full Adder**.
- Developed **Test Bench architecture.**
- Implemented **Callback in test bench architecture to drop and pass the generated transactions**.
- Developed **System Verilog based environment** for the same and verified the DUT.

Languages: Verilog, System Verilog Tools: VCS

B.Tech Project: Some Studies on Multi Band Frequency Selective Surfaces. **2018 - 2019**

Description: This project involves **design of multi band FSS filters** and studying their performance and other parameters for **wireless applications**.

Tools: HFSS 13.0 (ANSYS)

Summer Intern Project: Design of Single Pipelined 128 bit AES Algorithm **May 2018 – July 2018**

Description: This project involves design of **single pipelined 128-bit Advanced Encryption Algorithm (AES). It is a highly secured and modern cryptographic algorithm.**

Roles & Responsibilities:

- Developed the **design for AES** by considering the standard specifications provided by the **National Institute of Standards and Technology (NIST).**
- Verified the design results using the **sample key and plain text given by the NIST**.

Languages: Verilog Tools: Xilinx ISE Design Suite

TECHNICAL SKILLS

Protocol Knowledge:	**AMBA AHB, UFS 2.0, RISC-V, DES, AES, RSA**
Programming Languages:	**C, Java, Python, git and svn.**
HDL & HVL:	**Verilog, System Verilog.**
Tools:	**VCS, Questa Simulator, Xilinx ISE Design Suite, Vivado, PyCharm.**
Methodology:	**UVM.**
Operating system:	**Mac, Linux/UNIX, Windows.**

EDUCATION 2015-2019

- **B-Tech** in **Electronics and Communication Engineering** from **National Institute of Technology, Sikkim** with a **CGPA** of **7.54 out of 10**.